Shuowei Li

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OBJECTIVE: To obtain a 2017 summer internship position in circuit design and optimization.

EDUCATION

University of Washington, Seattle, WA
Doctor of Philosophy in Electrical Engineering — Ph.D. Advisor: Prof. Richard C. J. Shi
Expected June 2019

University of Washington, Seattle, WA
Bachelor of Science, Electrical Engineering — Sept. 2010 – June 2014
Concentration: VLSI Design, Embedded Computing Systems — Major GPA: 3.7/4.0

SUMMARY OF QUALIFICATIONS

- Ph.D. student concentrates in mixed-signal design and optimization
- Relevant Course: Advanced RF IC Design, Automatic Layout of Integrated Circuits, Communication Theory, Digital Signal Processing, Data Structure, Algorithms, Numerical Methods for Circuit Simulation
- Skills: Cadence/ADS, Verilog-A (AMS), SKILL, Python, C/C++, Verilog, MATLAB/Simulink, Java

WORKING EXPERIENCE

Research Intern, **Samsung Research America**, Richardson, TX — June 2016 - Sept. 2016

- Designed class-E power amplifier, including driver stage and impedance matching networks
- Achieved DC-RF efficiency of 74% at 5.8 GHz with transmitting power of 30 dBm
- Responsible for the entire design flow, including FCC compliant research, schematic/layout level design, and post-silicon testing

Teaching Assistant, EE 475 Senior Design Capstone: Design of Computer Subsystem — 2014 -2016

- Guided students in high speed digital design in Verilog and I/O interface design in C
- Responsible for leading lab sections of 30 students, giving lecture presentations and setting design goals

Research Intern, **National University of Singapore**, advised by Prof. Ellen Yi-Luen Do — Summer 2014

- Complemented PCB design and classification/algorithms implementation of CaRing, which provides real-time sensing of hand postures to prevent Carpal Tunnel Syndrome.

RESEARCH EXPERIENCE

Silicon Systems Research Laboratory, advised by **Prof. Richard C.J. Shi**

Capacitor Array Synthesizer for SAR-ADC

- Worked on array structure synthesis and layout optimization under symmetry/mismatch constraints
- Proposed an optimized layout synthesis flow that interacts with the EDA tool via the SKILL language to automatically generate the netlist and layout of the capacitor array

PROJECT EXPERIENCE

CMOS RF Receiver Front-end of WCDMA in TSMC 90nm, EE 536 Advanced RF IC Design — Spring 2015

- Designed and optimized a WDMA RF receiver frontend, including LNA, VCO and mixer
- Post layout simulation yielded LNA S11 = -15.3dB, VCO phase noise = -156.5 dBc/Hz, mixer conversation gain = 20.5dB. Receiver chain NF = 5.55dB, IIP3 = -11.1dB

SPICE-like Circuit Simulator, EE 537 Computation Methods for Circuit Analysis and Simulation — Spring 2015

- Developed a SPICE-like circuit simulator that performs DC and time-domain circuit simulation

EE 541 Automated Layout of Integrated Systems — Autumn 2015

- Implemented various EDA algorithms, including Fiduccia-Mattheyses partitioning, variable node size sliceable floor planning, simulated annealing placement, maze router based global routing, and left-edge channel routing